Semi-classical modeling of nanoscale nMOSFETs with III-V channel

Pierpaolo Palestri[1], Enrico Caruso[2], Oves Badami[3], Francesco Driussi[1], David Esseni[1], Luca Selmi[4]
[1]DPIA, University of Udine, Italy, pierpaolo.palestri@uniud.it
[2]Tyndall National Institute, Ireland, [3]University of Glasgow, [4]DIEF, Università di Modena e Reggio Emilia, Italy

Abstract

We review recent results on the modeling of nanoscale nMOSFETs with III-V compounds channel material. The focus will be on semi-classical transport modeling in short channel devices; we will show that back-scattering in the channel still influences the device performance, and thus affects the choice of the channel material. The model ingredients necessary to describe III-V MOSFETs will be discussed, and major differences compared to modeling of silicon FETs will be highlighted.

(Keywords: Simulation, Monte Carlo, III-V compounds)

Introduction

Over the last decades, there has been a significant interest in using III-V semiconductors as replacement of silicon in the channel of nanoscale nMOSFETs [1]. This has been mainly driven by the high mobility and high electron velocity associated to the small effective mass of the Γ valley in these materials, which may allow to achieve on-currents (I_{ON}) comparable to those of silicon devices but at a lower supply voltage, thus saving on the dynamic power of digital circuits [2]. Significant modeling efforts should flank the interpretation of experimental results and device optimization due to the large number of possible combinations for compounds/alloys, gate stacks and device structures [3]. In this paper, we review the main features of the semi-classical modeling for n-type MOSFETs and show sample applications to different III-V channel materials and device architectures.

Main modeling ingredients

Many properties of III-V compounds make most of the models developed for silicon devices inadequate for nanoscale III-V MOSFETs.

Firstly, as those materials are intended for ultimately scaled MOSFETs, control of short-channel-effects requires the use of ultra-thin-body or finFET / gate-all-around structures, where carrier quantization cannot be neglected. Differently from silicon, quantization does not only imply a shift of the band minima: the effective masses and non-parabolicity coefficient are also appreciably modified [4], which demands quantization models going beyond the effective mass approximation.

Another important aspect is related to the low density of states (DoS) of the Γ valley that drives the Fermi level well inside the bands, and makes it mandatory to use Fermi-Dirac statistics in close to equilibrium conditions, and to account for final states occupation in the numerical solution of the Boltzmann-Transport-Equation (BTE). The low DoS has an impact on the device electrostatic, and thus influences the "effective gate length" of the device [5].

In most III-V semiconductors, many valleys contribute to high-field transport. Their combined effect is observed in velocity-field characteristics [6], where at high longitudinal field L-valleys with high effective mass are populated thus reducing the average velocity.

Among the different approaches to model transport MOSFETs with III-V channels, we focus here on the semi-classical Multi-Subband approach [7]. In this approach, the description of quantization normal to transport directions is decoupled from the description of transport by solving a set of coupled BTEs for the low dimensional electron gas. The numerical solution may be obtained, for instance, via a Multi-Valley Multi-Subband-Monte-Carlo (MV-MSMC) method. This has been extensively used for planar FETs (e.g. UTB double-gate devices), where a 1D quantization problem is solved in each device slice normal to the transport plane, and then subband profiles and wave-functions are used to solve the BTE for the 2D electron gas [7]. Similarly, for 3D devices such as nanowires, one can solve a 2D quantization problem and then use a 1D BTE solver for transport [8].

The semi-classical approach is not fully adequate for the subthreshold region, where source-to-drain and band-to-band tunneling can be significant [9] (although workarounds can be implemented to improve its accuracy [10]). On the other hand, it allows for the inclusion of complex scattering mechanisms that are necessary for evaluation of the different technology options.

Results

Fig.1 reports the simulated velocity - field curves for GaSb, where the energy offset between Γ and L valleys is very small, so that both valleys contribute to transport even at low fields.

Fig.2 shows the simulated current for a nanoscale double-gate $In_{0.53}Ga_{0.47}As$ MOSFET. The on-current is very large in the ballistic limit and also when phonon scattering alone is considered, according to the large

mobility of the bulk material. On the other hand, inclusion of surface roughness scattering according to the recently proposed non-linear model [12] predicts a significant current reduction.

The relevance of scattering when assessing new material options is analyzed in Fig.3, where we consider strained (111)-GaAs and (111)-GaSb. These materials are interesting because of the relatively high DoS due to contributions by the L-valley [14][15]. In ballistic transport conditions, this results in an increased current and mitigates the 'DoS bottleneck' [16]. Unfortunately, the higher DoS also results in higher scattering rates: even by considering phonons alone, the current is much lower than the ballistic limit and close to the one of the device in Fig.2 simulated with phonons. Surface roughness further reduces the on current.

Beside scattering, other relevant effects reducing the current of III-V MOSFETs are traps in the gate dielectric, interface states and series resistance. The defectivity of the high-k/III-V interface is in fact worse than at the Si/SiO_2 interface. Accurate models are available in commercial TCAD to simulate the C-V characteristics of MOS capacitors with interface and border traps [17]. An example of C-V dispersion is shown in Fig.4. If the same trap profile is used in the MV-MSMC, the I_{ON} of the device in Fig.2 is reduced by ~11% w.r.t. simulations that include all scattering mechanisms, due to the additional scattering and Fermi-level-pinning (reducing the inversion charge [19]).

Concerning series resistance, largely dominated by contact resistance, the contact resistivity ρ_C of metal/InGaAs is slightly lower than the one of NiSi/Si for the same doping (see Fig.5). However, it is very challenging to attain high doping levels in the source and drain of III-V transistors, that results in an overall contact resistance larger than in Si devices. Even if we consider to meet the ITRS requirements for R_{SD}, the inclusion of the associated voltage drop lowers the I_{ON} of the device in Fig.2 by ~20% w.r.t. the curve "all. scat. mech.". Fig.5 also shows calculated ρ_C with a model for thermionic emission and tunneling through the image-force lowered barrier, accounting for non-parabolicity.

Finally, as an example of results for 3D structures using a deterministic solution of the BTE, we show in Fig.6 how the I_{ON} of stacked InGaAs nanowires is reduced by surface roughness.

Conclusion

The accurate description of state of the art nanoscale III-V devices requires mastering quantum mechanical, semiclassical and TCAD modeling approaches since many factor concur in determining the drive current. Among these, we underline the importance of carrier scattering, which still plays an important role for the proper selection of the channel material and device architecture.

Acknowledgments

The authors gratefully acknowledge funding from the E.U. (project III-V-MOS) and support from P. Hurley, D. Lizzit and P. Osgnach.

References

[1] J. A. del Alamo, Nature, v. 479, p. 317, 2011, doi: 10.1038/nature10677
[2] ITRS, 2013
[3] L.Selmi at al., Proc. IEDM, 2017, p.322.
[4] G. Zerveas et al., Solid-State Electron., v. 115, p. 92, 2016, doi: 10.1016/j.sse.2015.09.005
[5] D. Lizzit, et al., IEEE Trans. Elect. Dev., v. 61, p. 2027, 2014, doi: 10.1109/TED.2014.2315919
[6] E. Caruso et al., in Proc. EUROSOI-ULIS 2017, p. 152, doi: 10.1109/ULIS.2017.7962587
[7] D. Esseni, P. Palestri, and L. Selmi, Nanoscale MOS Transistors: Semi-Classical Transport and Applications, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 2011
[8] O. Badami et al., IEEE Trans. on Elect. Dev., v.65, p.2646, 2018, doi: 10.1109/TED.2018.2857509
[9] M.Rau et al., Proc. IEDM, 2016, p.758
[10] P. Palestri et al., Semic. Sci. Tech., v. 25, p. 055011, 2010, doi:10.1088/0268-1242/25/5/055011
[11] W. Jantsch et al., Phys. Rev. B, v. 3, p. 420, 1971, doi : 10.1103/PhysRevB.3.420
[12] D. Lizzit, et al.,J. Appl. Phys., v. 116, p. 223702, 2014, doi: 10.1063/1.4903768
[13] E. Caruso et al., IEEE Trans. Elect. Dev., v. 63, p.4685, 2016, doi: 10.1109/TED.2016.2612643
[14] M. Rodwell et al., Proc. DRC, 2010, p. 149.
[15] K. Alam et al., IEEE Trans. Elect. Dev., v. 61, p. 1335, 2014, doi : 10.1109/TED.2014.2311840
[16] M. Fischetti et al.," Proc. IEDM, 2007, p. 109.
[17] E. Caruso et al., in Proc. EUROSOI-ULIS 2018.
[18] Sentaurus Device User Guide, Synopsys Inc., Mountain View, CA, USA, 2014.
[19] P. Osgnach et al., Solid-State Electron., v. 108, p. 90, 2015, doi: 10.1016/j.sse.2014.12.011
[20] A. Baraskar et al., in Proc. IPRM, p.196, 2012
[21] N. Stavitski et al., IEEE Elect. Dev. Lett., v. 29, p.378, 2008, doi: 10.1109/LED.2008.917934

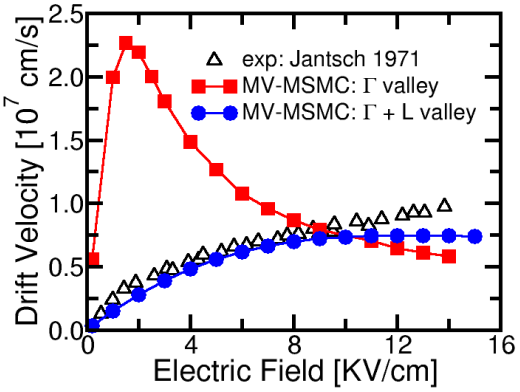

Fig.1 Simulated velocity-field curve for bulk GaSb. Results from MV-MSMC are compared with the experiments in [11].

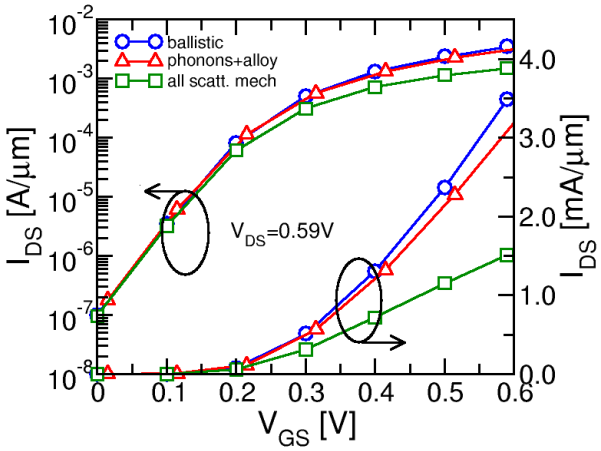

Fig.2 Simulated (MV-MSMC) current for a DG $In_{0.53}Ga_{0.47}As$ MOSFET with Lg=10.4nm, Tw=4 nm.

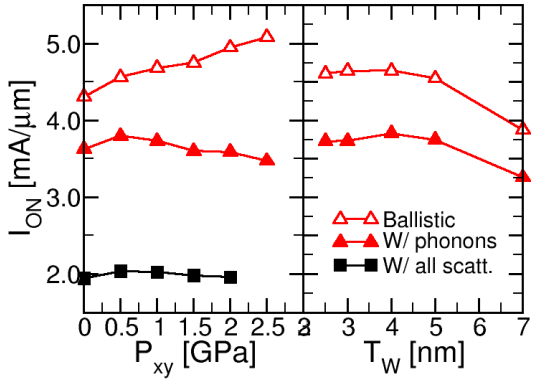

Fig.3 Simulated (MV-MSMC) current for (left) (111)-GaAs double-gate MOSFET with Lg= 15 nm and Tw=5 nm as a function of strain [13] and (right) (111)-GaSb double-gate MOSFET with Lg=15 nm and varying Tw. In the right plot the S/D doping is increased when reducing Tw in order to keep the same total dose and contain source starvation [16].

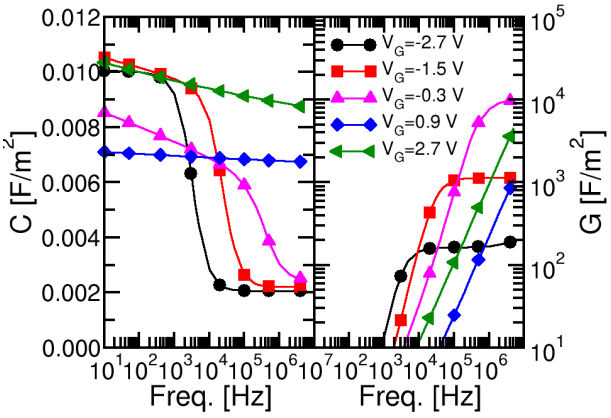

Fig.4 Simulated [18] capacitance and conductance vs frequency for a stack of 6nm Al_2O_3/2 μm $In_{0.53}Ga_{0.47}As$/InP. The trap distribution has been adjusted on experiments (not shown).

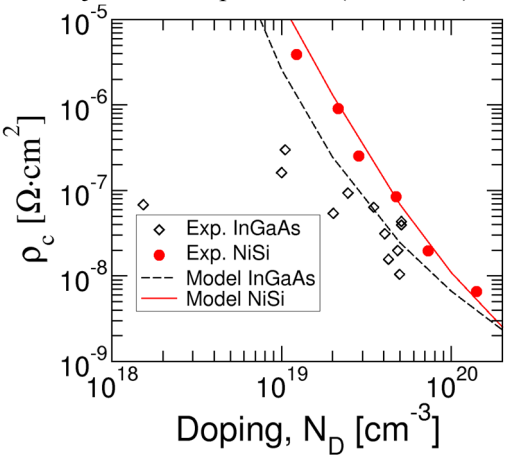

Fig.5 Measured contact resistivity for metal on $In_{0.53}Ga_{0.47}As$ [20] and NiSi on Si [21] compared with a model for thermionic emission and tunneling at the MS junction. SBH=0.5eV (0.6eV) for NiSi/Si ($In_{0.53}Ga_{0.47}As$).

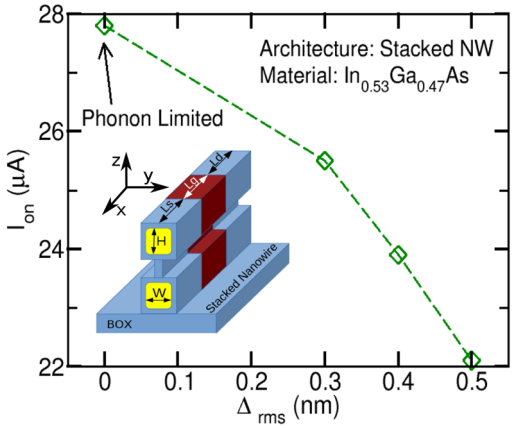

Fig.6 Simulated (deterministic-BTE) I_{ON} vs r.m.s. value of surface roughness for stacked $In_{0.53}Ga_{0.47}As$ nanowires. Details of the structure in [8].